Reducing Noise and Distortion in a Receiver System

DESCRIPTION

(Para 1) Related Application

The present application is related to the co-pending application entitled, "High Order Trans-impedance Filter with a Single Operational Amplifier", naming as inventors CHANDRA *et al*, filed on even date herewith, attorney docket number: TI-38003, serial number: UNASSIGNED, and is incorporated in its entirety herewith.

(Para 2) Background of the Invention

(Para 3) Field of the Invention

(Para 4) The present invention relates to communication systems, and more specifically to a method and apparatus to reduce noise and distortion in a receiver system.

(Para 5) Related Art

(Para 6) Receiver systems (e.g., wireless or wired systems) receive signals from various sources, and process the received signal to recover the information encoded in the received signals. In general, a signal of interest (e.g., encoding the information) is present in a frequency band of interest of the received signals. The received signals typically also contain unwanted signals outside of the frequency band of interest.

(Para 7) The signals of interest (when received at receiver systems) are often weak due to factors such as distance between a transmitter (sending the signals) and the receiver, the strength with which the transmitter generates the signals, etc. Such a weak signal needs to be amplified with filtering before processing, at least to avoid the effect of strong interference signals, which have frequencies adjacent (close) to the frequency band of interest.

(Para 8) In general, receiver systems perform various operations such as amplification and filtering to amplify the weak signals of interest and to remove the remaining unwanted signal components. The generated amplified signal of interest is provided for further processing. Due to the operations (amplification and filtering), the effect of interference signal may be avoided.

(Para 9) Such operations generally need to be implemented while meeting various objectives. One such objective is to minimize/avoid introduction of additional

noise (into the signal of interest). Noise refers to an undesirable signal component introduced along with (or into) the signal of interest, and is often formed/introduced by components which perform the operations.

(Para 10) Another objective while performing such operations is minimize/avoid introduction of additional distortion. In general, when the input signal is subject to operations such as amplification, there needs to be a linear response (e.g., same amplification factor during amplification operation). Deviations from the linear response (or any desired response, in general), is referred to as distortion. By minimizing the distortion, the resulting (amplified) signal would accurately represent the information in the signal of interest.

(Para 11) One source of such distortion (non-linearity) is the non-linear characteristics of components such as transistors. For example, transistor clips the peak voltage of the received (or amplified) signals if the voltage swing is large. However, a large voltage swing is desirable to reduce the effect of noise, and a low voltage swing is desirable to reduce distortion.

(Para 12) What is therefore required is a method and apparatus to reduce both noise and distortion in receiver systems.

(Para 13) **Brief Description of the Drawings**

(Para 14) The present invention will be described with reference to the following accompanying drawings.

(Para 15) Figure (Fig.)1 is a block diagram of an example receiver system in which several aspects of the present invention are implemented.

(Para 16) Figure 2 is a circuit diagram illustrating the details of a mixer in one prior embodiment.

(Para 17) Figure 3 is a circuit diagram illustrating the details of a filter circuit in one prior embodiment.

(Para 18) Figure 4 is a logical diagram illustrating the noise/distortion caused by the combination of the mixer of Figure 2 and filter circuit of Figure 3 in an embodiment.

(Para 19) Figure 5A is a circuit diagram implemented in single-ended mode illustrating the details of a combination of a mixer and a filter circuit in an embodiment of the present invention.

(Para 20) Figure 5B is a circuit diagram implemented in differential mode illustrating the details of a combination of a mixer and a filter circuit in an embodiment of the present invention.

(Para 21) Figure 6A is a circuit diagram implemented in single-ended mode illustrating the details of a second order filter circuit in an embodiment of the present invention.

(Para 22) Figure 6B is a circuit diagram implemented in differential mode illustrating the details of a second order filter circuit in an embodiment of the present invention.

(Para 23) Figure 7 is a graph illustrating the impedance characteristics of a second order filter with the frequency values shown on X-axis and the input impedance value shown on Y-axis in an embodiment of the present invention.

(Para 24) Figure 8 is a graph comparing the noise characteristics of embodiments of prior art with the example embodiments according to various aspects of the present invention.

(Para 25) Figure 9A is a circuit diagram illustrating a general form of the filter circuit in single-ended mode according to an aspect of the present invention.

(Para 26) Figure 9B is a circuit diagram illustrating a general form of the filter circuit in differential mode according to an aspect of the present invention.

(Para 27) Figure 9C is a circuit illustrating a modification to the differential circuit of Figure 9B which provides a designer more design choices in achieving desired filter characteristics.

(Para 28) Figure 10 is a graph illustrating the feedback factor values corresponding to various input impedance values in one embodiment.

(Para 29) In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

(Para 30) Detailed Description

(Para 31) 1. Overview

(Para 32) A receiver system according to an aspect of the present invention contains a mixer which down-converts a received signal into an intermediate signal with the frequency band of interest centered at a lower frequency than that of the received signal, and provides the intermediate signal in the form of electric current. A filter then operates on the intermediate signal in the form of electric current to remove the unwanted interference signals.

(Para 33) As mixers can be implemented to generate intermediate signals of high current swing and filters can be implemented to process such signals, the effect of any noise introduced by filter can be reduced (since the noise component may be a small in magnitude compared to the high current swing). In addition, the voltage levels at the outputs of transistors in mixers can be ensured to be low in spite of the

high current levels. As the transistors generally operate linearly at low voltage levels, low distortion may also be obtained. Due to the low distortion, a high amplification factor can be used in generating the intermediate signals, further enhancing the noise immunity.

(Para 34) In addition, due to generation of the intermediate signals in the form of electric current, the effective voltage level even in the presence of strong interference signals, can be maintained to be low. The filter circuits can then be designed to filter the interference signals, as well as provide amplified signals of interest in voltage domain. As strong interference signals are not amplified in the voltage domain, the active components in filter circuits may be provided input signals with low voltage levels. Due to the linear operation of active components at low voltage levels, amplified signals of interest may be generated without being affected by any strong interference signals.

(Para 35) In an embodiment described below, the filter circuit is designed to generate an amplified signal in the voltage domain. In such an embodiment, the unwanted interference signals are removed by the filter circuit before providing the amplified signal in the voltage domain with a high voltage swing. Since the interference signals are not amplified in the voltage domain, even strong interference signals may not affect the information in the signals of interest.

(Para 36) Various aspects of the present invention are described below with reference to an example problem. Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the invention.

(Para 37) 2. Receiver System

(Para 38) Figure 1 is a block diagram of receiver system 100 illustrating an example system in which the present invention may be implemented. For illustration, it is assumed that receiver system 100 is implemented within a Wireless Local Area Network (WLAN) Receiver. However, receiver system 100 can be implemented in other devices (wireless as well as wire-based communications) as well.

(Para 39) Receiver system 100 is shown containing low noise amplifiers (LNA) 110, mixer 120, filter circuit 160, and analog to digital converter (ADC) 170. Each block/stage is described in further detail below.

(Para 40) LNA 110 receives signals on path 101 and amplifies the received signals to generate a corresponding amplified signal on path 112. For example, in wireless systems, the signals that are transmitted from satellites, etc. may be received by an antenna (not shown) and the received signals are provided on path 101. The received signals may be weak in strength and thus amplified by LNA 110 for further processing.

(Para 41) Mixer 120 may be used to down-convert the received amplified signal on path 112 into an intermediate signal with the frequency band of interest centered at a lower frequency than the carrier frequency of the received signal. In an embodiment, a signal with the frequency band of interest centered at 2.4 GHz (carrier frequency) is converted to a signal with the frequency band of interest centered at zero frequency.

(Para 42) Mixer 120 may receive the amplified signal on path 112 and a signal of fixed frequency on path 122 as inputs, and provides the intermediate signal on path 126. The signal of fixed frequency on path 122may be generated by a phase locked loop (not shown) in a known way.

(Para 43) Filter circuit 160 may correspond to a low pass filter which allows the desired low frequencies and rejects all other unwanted high frequencies present in the signal received on line 126. The filtered signal, which contains the frequency band of interest, is provided on path 167. ADC 170 converts (samples) the filtered signal received on path 167 to a corresponding digital value, which represents the signal of interest in received signal 101. LNA 110 and ADC 170 may be implemented in a known way.

(Para 44) It may be noted that some of the components (for example mixer 120 and filter circuit 160) described above may introduce noise and distortion in received signal 101, which is undesirable.

(Para 45) An aspect of the present invention reduces such noise and distortion in the receiver systems by having mixer 120 provide the intermediate signal to filter circuit 160 in the form of electric current (as opposed to in voltage domain). In general, an output signal (here, intermediate signal) would be deemed to be generated in the form of electric current if the percentage of change/swing of the magnitude of electric current (of the output signal) is (substantially) more than the

percentage of change of the magnitude of the voltage level (of the output signal) for the same change in an input signal.

(Para 46) It may be helpful to first understand the details of a prior mixer and filter circuit, which does not include one or more features of the present invention. Accordingly, prior mixer is described below first with reference to Figure 2.

(Para 47) 3. Prior Mixer

(Para 48) Figure 2 is a circuit diagram illustrating the details of a mixer in one prior embodiment. Mixer 200 is shown containing NMOS transistors 210, 220 and 230, and resistors 240 and 250. Each component is described below.

(Para 49) As noted above, mixer 200 converts input signal received on path 201 into an intermediate signal with the frequency band of interest centered at a lower frequency than that of the input signal. Such a conversion may be performed by multiplying the input signal with a fixed frequency signal as is well known in relevant arts. The manner in which the multiplication operation is performed by the circuit of Figure 2 is described below.

(Para 50) Transistors 210, 220 and 230 together operate to generate currents on paths 225 and 234, with each current representing the intermediate signal with a frequency band of interest centered at a lower frequency (0 in one embodiment). The currents are generated based on input signal 201 and the fixed frequency signals received on paths 202 and 203. The signals on paths 202 and 203 are same in magnitude and opposite in phase. The manner in which the intermediate signal may be generated is described below.

(Para 51) Transistor 210 receives input signal 201 on the gate terminal and provides a current (on path 211) which is proportionate to the voltage level of input signal 201. Such an operation may be attained by implementing transistor 210 to operate as a current source.

(Para 52) Transistors 220 and 230 receive a fixed frequency signal on the respective gate terminals 202 and 203. Transistors 220 and 230 are turned on/off based on the voltage level of signals 202 and 203 respectively. Since signals 202 and 203 are opposite in phase, when one of transistors 220 and 230 is turned on, the other one is turned off. hen transistor 230 is on, current on path 234 equals the current on path 211 and when transistor 230 is off, no current flows on path 234. Therefore, it may be noted that the current on path 234 is controlled by signal 203 (which controls the operation o transistor 230) and signal 201 (which controls the

current on path 211). Similarly, the current on path 225 is controlled by signals 202 and 201.

(Para 53) As a result, the currents on paths 225 and 234 represent the multiplication of input signal 201 with the fixed frequency signals 202 and 203 respectively. However, the frequency of the currents on paths 225 and 234 depends on the frequency of input signal and the fixed frequency signal.

(Para 54) In an embodiment, each of signals 202 and 203 is in the form of a square wave for ease of converting the input signal into the intermediate signal. A square wave may be viewed as containing multiple frequencies of sine wave signals. As a result, the current on paths 225 and 234 contains the intermediate signal with multiple sine wave signals of different harmonic frequency components including the frequency component (the component of interest) representing the difference of the carrier frequency of the input signal and the fundamental frequency of the fixed frequency signal (paths 202 and 203).

(Para 55) In the example embodiment noted above, the intermediate signal is generated with a lower frequency equaling zero by selecting the frequency of signals 202 and 203 equaling the center frequency (the frequency at which the frequency band of interest is centered) of input signal 201.

(Para 56) Resistors 250 and 240 respectively convert electric currents 225 and 234 into corresponding voltage signals, which are required to interface with a prior filter circuit (described in sections below). The intermediate signal on path 299 is provided in the form of electric voltage to a filter circuit. The description is continued with reference to a prior filter circuit.

(Para 57) 4. Prior Filter Circuit

(Para 58) Figure 3 is a circuit diagram illustrating the details of a filter circuit in one prior embodiment. Filter circuit 300 operates as a second order low pass filter (LPF) and is shown containing operational amplifier 310, resistors 320, 330, 340, and 350, and capacitors 360 and 370. Each component is described below.

(Para 59) Operational amplifier 310 receives the signal on path 311 at inverting input terminal through the path containing resistors 320 and 330. The non-inverting input terminal 312 is connected to ground to provide single ended operation. Operational amplifier 310 amplifies the signal at inverting input terminal 311 and provides the amplified signal on output path 399.

(Para 60) Resistors 320, 330, 340 and 350, and capacitors 360 and 370 together form a second order low pass filter circuit to allow only the frequency band of interest and reject all other frequency components in the signal received on path 299. Thus, filter circuit 300 may reject the unwanted interference signals in signal 299 and provides the filtered signal on path 399.

(Para 61) Assuming that the resistance of resistors 320, 330, 340 and 350 equal R4, R2, R1 and R3 respectively, and capacitances of capacitors 360 and 370 equal C2 and C1 respectively, the transfer function (H(s)) of filter circuit 300 is given by equation (1) below, wherein '*' and '+' respectively represent multiplication and addition arithmetic operations, and 's' represents jw in Laplace Domain.

$$H(s)=\frac{R_3}{R_4}\cdot\frac{1}{1+sC_2\cdot(R_3+R_2+\frac{R_3R_2}{R_1}+\frac{R_3R_2}{R_4})+s^2\cdot C_1C_2R_3R_2}..........Equation(1)$$

(Para 62) It may be observed that the gain of the filter circuit depends on ratio R3/R4. However, resistors R3 and R4, along with other resistors (R1, R2) introduce noise in the signals of interest. The problems with prior mixer 200 and prior filter circuit 300 are described below with reference to Figure 4.

(Para 63) 5. Problems with Prior Embodiment(s)

(Para 64) Figure 4 is a circuit diagram containing a logical view of combination of mixer 200 and filter circuit 300 in an embodiment. Only some of the components in mixer 200 and filter circuit 300, as relevant to illustrate the problems are shown in circuit 400. In particular, various capacitors (which may otherwise be present) are not shown, and thus the logical diagram represents a circuit operating at low frequencies. Even though, the analysis that would be made based on the logical diagram may not provide accurate results, the results were empirically found to be within 10-15% accuracy.

(Para 65) Mixer 200 is shown containing resistor 240 and current source 440. Current source 440 represents the current (In_mix) due to noise components in mixer 200. Filter circuit 300 is modeled as operating at a low frequency and thus capacitors 360 and 370 are not shown. It may be noted that resistors 320, 330, 340 and 350 are connected in a star fashion (connected to a single electrical node) and the delta equivalent (containing resistors 420 and 430) of the resistors is shown in Figure 4. Accordingly, the values of resistors 420 and 430 respectively represented by Ra and Rb are given by Equations (2) and (3) below.

(Para 66) Ra = R2+(R4||R1) + R2(R4||R1)/R3 .... Equation (2)

(Para 67) Rb = R2+R3+R2R3/(R4||R1) .... Equation (3)

(Para 68) wherein ' II' represents parallel connection between resistors of corresponding resistance values on both sides of ' II' . For example, R_4 II R_1 equals $R_4 * R_1/(R_4+R_1)$.

(Para 69) Voltage source 450 represents the noise introduced by operational amplifier 310. The output voltage on path 399 due to noise components in circuit 400 is given by equation (4) below.

$$V_n^2 = \left(\frac{i_{n,mix} R_b R_L}{R_a + R_L}\right)^2 + v_{n,amp}^2 \left(1 + \frac{R_b}{R_a + R_L}\right)^2 + 4kTR_b\left(1 + \frac{R_b}{R_a + R_L}\right) \text{.......} Equation(4)$$

(Para 70) wherein R_L represents the resistance of resistor 240, k is Boltzman' s constant (well known in the relevant arts), and T is ambient/room temperature in absolute/Kelvin scale.

(Para 71) It may be appreciated that Equation (4) has three components separated by the + signs, and first component, second component and third component respectively represent the noise voltages due to mixer 200, operational amplifier 300 and resistors in filter circuit 300.It may be noted that the signal on path 299 is in the form of electric voltage and resistor 420 (R_a) converts voltage 299 into the corresponding electric current for proper operation of filter circuit 300. R_a needs to be large to interface with mixer 200 (which provides a signal in the form of voltage on path 299) since a low value of R_a may cause loading effect on mixer 200 resulting in (undesirable result of) reduction of voltage level of voltage 299. A high value of Ra in turn increases the noise level since several resistors in a filter circuit may also need to be scaled up correspondingly.

(Para 72) The ratio R_b/R_a represents the gain of filter circuit 300 of Figure 4, which is fixed based on the gain requirement of the filter circuit at the specific operation time instance. Therefore, by observing components 2 and 3 of Equation (4), it may be observed that the noise due to operational amplifier 300 and resistors in the filter circuit is amplified by the gain of the filter circuit, further resulting in increase of the noise when a higher gain is sought, which is undesirable. Hence, one problem with prior filter circuit 300 is the introduction of noise in the filtered signal provided on path 399.

(Para 73) The noise due to resistors can be reduced by reducing the resistance values of resistors 420 and 430. However, to maintain the desired response of the filter, the reduction in resistance values requires an increase in the capacitance values of capacitors in filter circuit 300 of Figure 3, which leads to increased area requirement and fabrication challenges. There is often also a limit to which resistance values can be reduced based on loading seen by mixer 200. Therefore, reducing resistance values may not be desirable, at least in some environments.

(Para 74) Alternatively, the effect of noise due to resistors 420 and 430 can be minimized by providing a signal with a high voltage swing on path 299. Due to such a high swing for the input signal, the strength of signal components can be made to be substantially more than the strength of the noise components, thereby causing the noise due to high resistance values to be negligible.

(Para 75) However, one problem with mixer 200 with the generation of high voltage swing signals on path 299 is that transistors 220 and 230 of Figure 2 may provide a non-linear response while processing signals with such a high voltage swing. The non-linear response would in turn cause distortion in the signal provided on path 299. The distortion in the signal would be worse if mixer 200 is implemented to operate at low supply voltages. However, there are several environments in which low supply voltages are desirable. Accordingly, use of high voltage swing on path 299 may be inadequate in some environments.

(Para 76) The manner in which one or more of the problems with prior mixer and filter circuit can be addressed according to various aspects of the present invention is described below.

(Para 77) 6. Modifying Prior Circuits for Low Noise/Distortion

(Para 78) An improvement to the combination of the mixer and filter circuit is based on an observation that a current to voltage conversion and then again a voltage to current conversion is performed in the combination circuit of Figure 4. The current to voltage conversion is performed by resistor 240, and the voltage to current conversion is performed by resistor 420. A current mode interface is provided between a mixer and a filter circuit according to an aspect of the present invention, which enables removal of resistor 240 in mixer 200 and resistor 420 in filter circuit 300. By removing resistor 420 (which is a source of the noise), noise introduced by the filter circuit can be reduced.

(Para 79) In addition, as current on path 234 is directly provided to the filter circuit, the requirement of large voltage swing on path 299 may be eliminated. The absence of large voltage swing on path 299 reduces distortion in the signals of interest. Thus, low noise and low distortion can be attained by using a current mode interface between the mixer and the filter circuit (as described with examples below).

(Para 80) However, removal of resistor to provide current mode interface in filter circuit may require redesign of the filter circuit at least to meet various parameters (Q-factor, frequency response, etc.,) as desirable.

(Para 81) The redesign may need to take into account other requirements as well. For example, an ideal current mode input circuit (i.e., filter which receives the current input) has to offer zero input impedance. Accordingly, it is desirable to implement the filter circuit (at least a first stage of the filter circuit) with a low input impedance to receive current from the mixer. Example mixer-filter circuits which meet some of such requirements are described below in further detail.

(Para 82) 7. Combination of Mixer and Filter circuit

(Para 83) Figure 5A is a circuit diagram illustrating the details of a combination of mixer and filter circuit implemented for single-ended mode of operation in an embodiment of the present invention. Mixer-filter circuit 500 is shown containing mixer 591 and filter circuit 592. Mixer 591 is shown containing NMOS transistors 510, 520, and 530, and current sources 540 and 550. Filter circuit 592 is shown containing capacitor 560, resistor 570 and operational amplifier 580. Each component is described below.

(Para 84) Mixer 591 is assumed to operate from input 112 and filter circuit 592 is assumed to operate from input 126 generated by mixer 591. Thus, the combination of mixer 591 and filter circuit 592 can be used in place of the combination of mixer 120 and filter circuit 160 of Figure 1. As noted above, mixer 591 converts input signal received on path 112 into an intermediate signal in the form of electric current with the frequency band of interest centered at a lower frequency than that of the input signal, and provides the electric current on path 126. The conversion may be performed by using fixed frequency signals on paths 502 and 503. Signals 502 and 503 are similar to signals 202 and 203 of Figure 2. Paths 502 and 503 are contained in path 122 of Figure 1.

(Para 85) Current sources 540 and 550 provide the current to set bias point for linear operation of transistors 510, 520 and 530. The magnitude of the current source may be determined accordingly. The determination of the magnitude and the implementation of current sources will be apparent to one skilled in the relevant arts. The common mode voltage between mixer 591 and filter circuit 592 is set by a common mode feed back loop (not shown) as is well known in relevant arts. For example, the common mode voltage is set to bias current sources 540 and 550, and operational amplifier 580 optimally.

(Para 86) One terminal of each of current sources 540 and 550 is connected to supply Vdd and the other terminal of each of current sources 540 and 550 is connected to the drain terminal of transistors 530 and 520 respectively. Transistors 530 and 520 receive fixed frequency signals on the respective gate terminals 502 and 503. The source terminals of each of transistors 530 and 520 is connected to

the drain terminal of transistor 510. Transistor 510 receives input signal 112 on the gate terminal and the source terminal of transistor 510 is connected to Vss or ground.

(Para 87) Transistors 510, 520, and 530 of mixer 591 operate similar to transistors 210, 220 and 230 of Figure 2. For condiseness, the description of the components is not repeated. Due to the operation of transistors 510, 520, and 530, the current provided on path 534 represents intermediate signal 126, which is provided as input to filter circuit 592.

(Para 88) Operational amplifier 580 is shown with inverting input terminal 511 connected to receive signal on path 126 and non-inverting input terminal 512 connected to Vss or ground. Resistor 570 and capacitor 580 are connected in parallel between inverting input terminal 511 and output terminal of operational amplifier 580 on path 167.

(Para 89) Operational amplifier 580 receives the signal on path 126 at inverting input terminal. Non-inverting input terminal 512 is connected to ground to provide single ended operation. Operational amplifier 580 amplifies the signal at inverting input terminal 511 and provides the amplified signal on output path 167.

(Para 90) Resistor 570 and capacitor 560 together form a first order low pass filter to allow only the frequency band of interest and reject all frequency components other than the frequency band of interest in the signal received on path 126. By appropriate selection of the component values of resistor 570 and capacitor 560 based on the desired corner frequency (which separates the frequency band of interest from the frequency components sought to be rejected), unwanted interference signals may be rejected effectively.

(Para 91) Thus, filter circuit 592 may reject the unwanted interference signals in signal 126 and provides the filtered signal on path 167, which contains the frequency band of interest centered at lower frequency. Filter circuit 592 provides filtered signal 167 in the form of electric voltage even though the input signal received on path 126 is in the form of current.

(Para 92) As noted above, filter circuit 592 needs to provide zero input impedance for current mode interface. It may be observed that the input impedance of filter circuit 592 is zero/low since no components are present between path 126 and inverting input terminal 511. Thus, filter circuit 592 performs filtering operation on intermediate signal 126 received in the form of electric current.

(Para 93) It may be noted that resistors (such as 420 of Figure 4) are eliminated in filter circuit 592, thus the noise introduced by filter circuit 592 is reduced. The output voltage (Vn^2) on path 167 due to various noise components in circuit 500 is given by equation (5) below.

$$V_n^2 = \left(i_{n,mix} R_f\right)^2 + v_{n,amp}^2 + 4kTR_f ....Equation(5)$$

(Para 94) wherein R_f represents the resistance value of resistor 570.

(Para 95) It may be appreciated from equation (5) that noise due to operational amplifier 580 and resistor 570 is not amplified and thus the noise is reduced compared to the noise of Figure 4 as given with equation (4) above.

(Para 96) Further, the effect of noise (due to filter circuit 592) may be reduced by increasing the amplification factor of mixer 591 since the current on path 126 can be amplified substantially. As a result, the effect of noise on the large current signal 126 may be reduced. In addition, due to the current mode interface between mixer 591 and filter circuit 592, voltage swing of intermediate signal 126 can be kept small and thus distortion due to non-linearity of transistors in mixer 591 may be reduced.

(Para 97) Also, strong interference signals may not affect the processing of signals of interest since strong (in voltage domain) interference signals are not further amplified in mixer 591 before providing intermediate signal 126 to filter circuit 592. However, filtered signal 167 is provided with large voltage swing (as desirable for the operation of ADC 170), which contains only signals of interest.

(Para 98) Figure 5B represents the filter circuit 500 of Figure 5A, implemented in differential mode. Resistor 593 (operating in complementing position to resistor 570 for differential operation) and capacitor 594 (operating in complementing position to capacitor 560) are shown added to provide the differential mode of operation. In addition, the differential inputs 581 and 582 (generated by mixer 591) may be viewed as logically contained in path 126 of Figure 1. The output signals 598 and 599 may be viewed as logically contained in path 167 of Figure 1.

(Para 99) It may be noted that filter circuits of Figures 5A and 5B are single order filters, which may not provide sharp frequency characteristics at cutoff frequency to reject interference signals. The interference signals due the absence of such sharp frequency characteristics can get amplified and presented at the output of filter circuit 592. Accordingly, a trans-impedance filter circuit of higher order, which

overcomes some of such problems, is described below with reference to Figures 6A and 6B.

(Para 100) 8. Second Order Trans-impedance Filter Circuit

(Para 101) Figure 6A is a circuit diagram illustrating the details of a second order trans-impedance filter circuit implemented for single-ended operation in an embodiment of the present invention. Filter circuit 600 is assumed to operate from input 126 generated by mixer 591 of Figure 5A. Thus, the combination of mixer 591 and filter circuit 600 can be used in place of the combination of mixer 120 and filter circuit 160 of Figure 1. Filter circuit 600 is shown containing resistors 610 and 620, capacitors 630 and 640, and operational amplifier 650. Each component is described below.

(Para 102) Intermediate signal 126 is shown provided to inverting input terminal 651 of operational amplifier 650 via resistor 610. One end of capacitor 630 is connected to receive the intermediate signal on path 126 and the other end is connected to Vss/ground. Resistor 620 is connected between path 126 and output terminal 167 of operational amplifier 650. Capacitor 640 is connected between inverting input terminal 651 and output terminal 167 of operational amplifier 650.

(Para 103) Operational amplifier 650 receives input signal 126 on path 651 on the inverting input terminal, as noted above. The non-inverting input terminal 652 is connected to ground to provide single ended operation. Operational amplifier 650 amplifies the signal at inverting input terminal 651 and provides the amplified signal on output path 167.

(Para 104) Resistors 610 and 620, capacitors 630 and 640 together form a second order low pass filter circuit to allow only the frequency band of interest and reject all other frequency components in the signal received on path 126. Thus, filter circuit 600 may reject the unwanted interference signals in signal 126 and provides the filtered signal on path 167.

(Para 105) The input signal 126 to filter circuit 600 is in the form of electric current (Iin)and filtered signal 167 is in the form of electric voltage (Vo). Assuming that the resistance of resistors 610 and 620 equal R and Rf, and capacitances of capacitors 630 and 640 equal C1 and C2 respectively, the transfer function of filter circuit 600 is given by equation (6) below.

$$\frac{V_o}{I_{in}} = \frac{R_f}{1 + sC_2 \cdot (R_f + R) + s^2 \cdot C_1 C_2 R_f R} \text{..........} Equation(6)$$

(Para 106) It may be noted from equation (6) that the transfer function contains 's^2' term, which represents second order filter. It may be further noted that the transfer function (Equation (6)) of filter circuit 600 is similar to the transfer function (Equation (1)) of filter circuit 300. Thus, filter circuit 600 operates as a second order low pass filter (LPF), which provides sharper frequency characteristics than a single order filter as is well known. Filter circuit 600 can be implemented to operate in differential mode also, as described below with reference to Figure 6B.

(Para 107) In comparison to Figure 6A, the circuit of Figure 6B contains resistor 660 (operating in complementing position to resistor 610 for differential operation), resistor 680 (operating in complementing position to resistor 620), capacitor 680 (operating in complementing position to capacitor 630) and capacitor 670 (operating in complementing position to capacitor 640) in addition. The input signals 581 and 582 are assumed to be generated by mixer 591 of Figure 5B. The output signals 691 and 692 may be viewed as logically contained in path 167 of Figure 1.

(Para 108) Filter circuit 600 offers low input impedance to provide current mode interface to mixer 591, in spite of the presence of resistor 610. At low frequencies, the impedance is nearly zero because the capacitors 630 and 640 do not conduct any current, and therefore the current that flows through resistor 610 is (close to) zero., due to virtual ground of the operational amplifier on inverting input terminal 651. However, at intermediate frequencies the input impedance depends on the capacitors 630 and 640, as these conduct some current. Thus, the input impedance depends on the frequency of the intermediate signal 126 (or combination of 581 and 582). However, it is still low compared to the embodiments of Figure 3, as described in further detail below with reference to Figure 7.

(Para 109) 9. Impedance Characteristics

(Para 110) Figure 7 is a graph illustrating impedance characteristics of example embodiments of filter circuit 600 of Figures 6A/6B (line 710) and filter circuit 300 of Figure 3 (line 750), with the frequency values shown on X-axis and input impedance shown on Y-axis. It may be observed that the input impedance of filter circuit 600 is generally lower than that of filter circuit 300 for similar frequencies, by comparing lines 710 and 750.

(Para 111) In one embodiment (described in further detail in section 10 below), peak input impedance (i.e., maximum values on lines 750 and 710) of filter circuits 300 and 600 respectively equal 600 ohms and 450 ohms. Metrics such as average would more accurately reflect the advantages of various aspects of the present invention. The average value from line 710 would be substantially lower than that of line 750, representing the benefits of the embodiment(s) represented

by Figure 7. In one embodiment, the average input impedance of filter circuits 300 and 600 respectively equal 250 ohm and 650 ohms.

(Para 112) Line 710 represents the change in input impedance value for various frequencies. It may be noted that the input impedance value is maximum at one frequency. The frequency corresponding to maximum input impedance value is referred to as the corner frequency (cutoff frequency) and is shown by 701, which differentiates the frequency band of interest from the undesirable frequencies in the received signal.

(Para 113) The change in input impedance is due to capacitors 630 and 640 as the impedance value of capacitor 630 depends on the frequency of input signal received on path 126. It may be observed that the input impedance value drops substantially low for frequencies other than for the corner frequency, especially in frequency band of interest.

(Para 114) It may be appreciated that even though the input impedance changes with the frequency, the value of the input impedance is low compared to the input impedance of filter circuit 300 of Figure 3. However, it may be noted that the input impedance of filter circuit 592 of Figures 5A/5B is low (almost zero) and is independent of the frequency of input signal 126 to the extent operational amplifier 580 is ideal.

(Para 115) The description is continued with respect to comparison of noise characteristics (between the prior embodiments and the embodiments provided according to various aspects of the present invention, described above) with reference to Figure 8 below.

(Para 116) 10. Comparison of Noise Characteristics

(Para 117) Figure 8 is a graph illustrating noise characteristics with the frequency values shown on X-axis and the corresponding noise power spectral density (PSD) (representing distribution of noise power over a frequency band) shown on Y-axis. Lines 810 and 850 represent the noise characteristics of filter circuits 300 and 600 respectively (in one embodiment).

(Para 118) It may be observed that both lines 810 and 850 are shown decreasing in noise value with the increase in frequency. However, line 810 is shown with low noise value than line 850 for any specific frequency of operation.

(Para 119) In one embodiment, mixer 200 is implemented with a DC load of 500ohms, and filter circuit 300 is implemented with a corner frequency of 11.5MHz (Mega hertz), pole-Q of 0.64 and the dc gain of 12dB, the component values of filter circuit 200 found to be R2=750ohms, R3=6Kohms, R4=1.5kohms, c1=19.1 pF (pico Farads), C2=2.2pF, and R1 is assumed to be open circuited for simplification of the analysis. It is observed that mixer-filter combination of Figure 4 (prior embodiments) with the above component values lead to a noise figure (providing a measure of the degradation in the signal to noise ratio, as is well known in the relevant arts) of 4.5dB.

(Para 120) However, the combination of mixer 591 and filter circuit 600 can be implemented to meet the parameters noted above with the component values of R=500 ohms, Rf=4k ohms, C1=19.8 pF and C2= 4.8 pF. It is observed that the combination leads to a noise Figure of 3.3dB, which is an improvement in the reduction of noise of 1.2dB. Thus, filter circuit 600 of Figures 6A/6B according to an aspect of the present invention provides low noise PSD than filter circuit 300 of Figure 3 in one prior embodiment.

(Para 121) It may be appreciated that various modifications may be made to the circuits of Figures 6A and 6B, without departing from the scope and spirit of various aspects of the present invention. The description is continued with respect to a general filter structure, according to an aspect of the present invention.

(Para 122) 11. General High Order Filter Circuit

(Para 123) One limitation of the circuits of Figures 6A and 6B is that the transfer function is constrained to be an all-pole transfer function. An all-pole transfer function is one where the numerator does not have any "s" terms, and is hence frequency independent. A number of useful filters (for example Elleptical filter), well-known to one skilled in relevant arts, cannot be synthesized with this limitation.

(Para 124) Figure 9A is a circuit diagram illustrating the details of a general high order filter circuit 900 provided according to an aspect of the present invention. Filter circuit 900 can be used in place of filter circuit 160 for the synthesis of more general class of filters. Filter circuit 900 is shown containing resistors 910, 915, 920, and 990, capacitors 930, 935, 940, 960 and 995, and operational amplifier 950. Each component is described below.

(Para 125) The combination of resistors 910 and 915 connected in series, couples the input signal received at node 901 (on path 126) to the inverting input terminal of operational amplifier 950. Resistor 920 is connected between the

output terminal of operational amplifier 950 and node 901. Capacitor 940 is connected across the output terminal and inverting input terminal of operational amplifier 950. Capacitor 960 is connected between the junction of connection of resistors 910 and 915, and the output terminal of operational amplifier 950.

(Para 126) The combination of capacitors 930 and 935 connected in series, is connected between the inverting input terminal of operational amplifier 950 and node 901. Resistor 990 is connected between the junction of capacitors 930 and 935, and ground. Capacitor 935 is connected between ground and the junction of resistors 910 and 915.

(Para 127) In an embodiment, each of capacitors 930 and 935 has a capacitance magnitude equaling C, and capacitors 925 and 960 respectively have capacitance of 2k(1 – ë)C and 2kCë (the four factors being multiplied). Resistors 910, 915, and 990 respectively have resistance of R, R and kR/2. The (feedback) capacitance of capacitor 940 is represented by Cf and the resistance of resistor 920 is represented by Rf. With these values and convention, the transfer function of filter circuit 900 is given by Equation (7) below:

$$\frac{V_o}{I_{in}} = \frac{R_f(s^2C^2kR^2+1)}{1+A_1s+A_2s^2+A_3s^3} \ldots\ldots\ldots\ldots Equation(7)$$

Wherein,

$$A_1 = 2RCk\lambda + 2RC_f + 2R_fCk\lambda + R_fC_f$$

$$A_2 = 2R_fRC_fC(k+1) + R^2C^2k + 2C_fCR^2k + 2R_fRC^2k\lambda$$

$$A_3 = C^2C_fR^2R_fk$$

(Para 128) It may be observed that filter circuit 900 provides a third order transfer function in the denominator. However, it can be shown that the third (real) pole is usually at a much higher frequency than the two complex poles for typical values. Accordingly, in practice, the circuit of Figure 9A provides second order filter characteristics.

(Para 129) Similar to in Figure 6B, the single ended approach of Figure 9A can be extended to differential implementation as well, and the corresponding circuit is depicted in Figure 9B. In comparison to Figure 9A, Figure 9B contains resistors 910-A, 915-A, 920-A and 990-A, capacitors 930-A, 935-A, 940-A, 960-A and 995-A, and paths 126-A and 169-A in addition, which respectively provide the complementary operation to resistors 910, 915, 920, and 990, capacitors 930, 935, 940, 960 and 995, and paths 126 and 169, as required for the differential operation.

(Para 130) The parameter values k and ë, and the ratio Cf/C can be varied to achieve the desired corner frequency and pole Q-factor. The corresponding component values can be approximately calculated by ignoring the S^3 term of Equation 7), or solved exactly using computer programs in known ways. The configuration of Figure 9B leads to a positive value of ë. Another aspect of the present invention enables a negative value of ë to be attained, thereby providing greater choices to a designer in attaining desired filter characteristics as described below with reference to Figure 9C.

(Para 131) Figure 9C is similar to Figure 9B except that a terminal of capacitor 960 is connected to non-inverting output terminal 169-A (instead of inverting output terminal 169 as in Figure 9B) and the terminal of capacitor 960-A is connected to inverting output terminal 169. Due to such a configuration, a negative value for ë is attained, as would be apparent to one skilled in the relevant arts.

(Para 132) In addition, if ë = 0 (removing capacitor 960 from Figure 9A), as capacitors 930/935 and resistors 990/910 are removed, the topology of Figure 9A (9B) reduces to the topology of Figure 6A (9B) (with an extra capacitor), consistent with the statement that the circuit of Figure 9A (9B and 9C) represents a general topology from which the topology of Figure 6A can be derived.

(Para 133) Also, the topologies of Figure 6A and Figure 9A (9B and 9C) operate as ideal trans-impedance configurations at low frequency of input signals. In addition, it may be observed from Figure 7 that the input impedance exhibits a band-pass transfer function at high frequencies, which peaks at the corner frequency (701) of the filter.

(Para 134) To provide ideal trans-impedance configuration, the input impedance of the filter has to be low even at high frequencies. The desired low input impedance may be obtained by reducing the ratio of the resistance values of resistors 610 to 620 in filter circuit 600 of Figure 6, and reducing the ratio of the resistance value of resistors 910 and 915 to 920 in filter circuit 900 of Figure 9. However, such reduction in ratios would cause a correspondingly reduced feedback factor, as may be appreciated from the below equations (8) and (9), that are presented only for filter circuit 600. As is well known, feedback factor of an operational amplifier is defined as the percentage of signal that is fed back in the negative feedback configuration. A reduced feedback factor reduces the effective bandwidth of the op-amp, which makes the circuit more sensitive to op-amp non-idealities.

(Para 135) The input impedance of filter circuit 600 is given by Equation (8):

$$Z_{in} = \frac{(sC_2R)R_f}{1 + sC_2 \cdot (R_f + R) + s^2 \cdot C_1C_2R_fR} \ldots\ldots\ldots\ldots\ldots\ldots.Equation(8)$$

(Para 136) The feedback factor of filter circuit 600 is given by Equation (9):

$$\frac{1}{\beta} = 1 + \frac{sR_fC_1}{1 + sC_2 \cdot (R_f + R) + s^2 \cdot C_1C_2R_fR} \ldots\ldots\ldots\ldots.Equation(9)$$

(Para 137) By observing Equations (8) an (9), it can be appreciated that the input impedance and feedback factor of filter circuit 600 follows a band-pass transfer function. The maximum values of these parameters are present at the corner frequency, as given by the below equations 10 (for input impedance) and 11 (feedback factor):

$$Z_{in}\Big|_{\max} = (R \parallel R_f) \ldots\ldots\ldots\ldots\ldots\ldots\ldots.Equation(10)$$

$$\frac{1}{\beta}\Big|_{\max} = 1 + Q^2(1 + \frac{R_f}{R}) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.Equation(11)$$

(Para 138) By examining Figure 6, it may be noted that the trans-impedance of the circuit is determined by resistor 620. But the input impedance is determined by the parallel combination of resistor 620 and 610, as noted in equation (10) above. So, for a given trans-impedance, to reduce the input impedance resistor 610 should be reduced. However, such a reduction in the resistance value of resistor 610 would result in decreased feedback factor, as seen from equation (11). This is an undesirable effect.

(Para 139) Figure 10 illustrates the feedback factor values (Y-axis) for corresponding input impedance values (X-axis) in one embodiment. It may be generally observed that the feedback factor reduces with a reduction of the input impedance value. However, it is generally desirable to have a high feedback factor and low input impedance. Thus, depending on the requirements of the specific situation, a compromise needs to be attained between the conflicting requirements, and a designer may choose corresponding parameter values.

(Para 140) From the above, it may be appreciated that, filter circuits of Figures 5A, 5B, 6A, 6B and 9 provide low input impedance, which is desirable for current mode interface. As a result of the current mode interface between mixer 120 and filter circuit 160, the need for large voltage swing on path 126 is eliminated, which results in improved linearity (reduced distortion). In addition, due to the current mode interface to filter circuits of Figures 5A, 5B, 6A, 6B, and 9 the

need for some resistors is eliminated, which results in reduction in noise in the signals of interest.

(Para 141) 12. Conclusion

(Para 142) While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.